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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,146	12/28/2001	Kyo Seop Choo	465-884P	5228

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EXAMINER	
QI, ZHI QIANG	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,146	CHOO ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 1 and 13, recitation ". . . a pixel electrode on the passivation layer to electrically connect the first, second and third line layers through each contact hole" in claim 1, and recitation ". . . forming a pixel electrode on the passivation layer to electrically connect the drain electrode and the first, second and third line layers through the contact holes" in claim 13, are not clear and indefinite, and it is impossible that such structure for the pixel electrode can display image. According to the Fig.5 of the specification; and according to the claim 2 that the first line layer is formed of the same material as a gate line, so that the first line layer is a gate line; and according to the claim 4 that the second line layer is formed of the same material as a data line, so that the second line layer is a data line. Therefore, the pixel electrode is connected to the gate line and the data line. The gate line is for driving TFT, and the data line is for transfer signal to display image via TFT. If the gate electrode of the TFT and the source

electrode or drain electrode of the TFT are connected together via pixel electrode, how the TFT can be working, so that the pixel electrode cannot display image. Therefore, the limitations in the claims are not clear and cannot tell how the LCD can be enabled to make such invention.

Claims 2-12 and 14-18 are dependent to the claims 1 and 13 respectively, so that all the dependent claims have the same deficiency set forth above.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 13-18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13, recitation ". . . forming a gate line on a substrate of the cell array region, simultaneously, and a first line layer on the substrate at the input line part; . . . forming a data line having source and drain electrodes at both sides of the semiconductor layer of the cell array region, simultaneously, and a second line layer on the first insulating layer of the input line part; . . .forming a reflective layer on the second insulating layer of the cell array region, simultaneously, and a third line layer on the second insulating layer of the input line part; . . ." are not clear and indefinite. Because forming a gate line or a data line or a reflective layer that is only forming one gate line or one data line or one reflective layer, so that how can be simultaneously to form one gate line or one data line or one reflective layer; and any signal input line can be a input line part, so that the gate line is a input line part and any LCD has a plurality of gate lines

and data lines (according to the specification the first line is the gate line, the second line is the date line and the third line is the reflective electrode), such that how is a gate line being formed simultaneously with a gate line. Similarly, how is a data line being formed simultaneously with a date line, and how is a reflective layer being formed simultaneously with a reflective layer.

Claims 14-18 are dependent to the claim 13, so that all the dependent claims have the same deficiency set forth above.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 8-14 of U.S. Patent No. 6,466,280 in view of US 6,528,357 (Dojo et al) and US 2002/0101398 (Fujita).

Although the conflicting claims are not identical, but they are not patentably

distinct from each other because the claims 8-14 of the patent US 6,496,238 have a very corresponding limitations claimed in the claims 1-18 of this application, and substantially they have the doctrine of obviousness-type double limitations. Especially, the claims 1 and 13 of this application, the limitations for the input line (electrodes) arrangement for an LCD device are covered by the claims 8-14 of the patent US 6,466,280.

For example, claims 1 and 13 of this application claimed an LCD and the method of for manufacturing an LCD having a cell array region and an input line part (the input line part can be any signal input lines such as gate lines or data lines) comprising: (concerning claim 1 and 13)

- a first line layer (gate line) formed on a substrate;
- a first insulating layer (gate insulating layer) formed on the substrate, having a contact hole therein located at the first line layer;
- a second line (data line) formed on the first insulating layer;
- a second insulating layer formed on the substrate, having respective contact holes therein located at the first and second line layers (the gate line and the data line layers);
- a third line layer (reflective electrode) formed on the second insulating layer;
- a passivation layer (a third insulating layer) formed on the substrate, having respective contact holes therein located at the first, second and third line layers (the gate line, date line and the reflective electrode);

- a pixel electrode on the passivation layer (the third insulating layer) to electrically connect the first, second and third line layers (the gate line, data line and the reflective electrode) through each contact hole;

(concerning claim 13)

- a semiconductor layer formed on the first insulating layer of the cell array region.

The claim 8 of the patent US 6,466,280 claimed a transflective LCD device comprising a second substrate having:

- a gate electrode (gate line) formed on the second substrate; and any LCD has a plurality of gate lines, and any gate line is a signal input line to input signal to the TFT, so that any gate line on the substrate is at the input line part;
- a first insulating layer (gate insulating layer) formed on the exposed surface of the second substrate while covering the gate electrode;
- a semiconductor layer formed on the first insulating layer;
- a source electrode and a drain electrode (forming the data line) overlapping one end portion of the semiconductor layer (also means the data line formed on the gate insulating layer);
- a second insulating layer formed the exposed surface of the first insulating layer while covering the source and drain electrode, having contact hole (also means the second insulating layer formed on the substrate and having contact hole);

- a reflective electrode (as a third line layer) formed on the second insulating layer;
- a third insulating layer (such as a passivation layer) on the reflective electrode and having contact hole (also means a passivation layer formed on the substrate and having contact hole);
- a first contact hole formed on a portion of the drain electrode; the reflective electrode (as a third line layer) connected to the pixel electrode through a second contact hole, that is the respective contact holes to expose the drain electrode and the third line layer; and concerning to expose the gate line and the data line (as a first and second line layer) that is the same principle as to expose the drain electrode and the reflective electrode using contact holes through insulating layer, and that have been at least obvious.
- a pixel electrode formed on the third insulating layer and electrically connected with the reflective electrode through contact hole.

Concerning the limitation such that the pixel electrode connected the drain electrode and the gate line, data line and reflective electrode (as a first, second and third line layers) through contact holes, as Fujita discloses (paragraph 0024 – 0025) that the drain electrode is connected to the drain region via a first contact hole formed in the gate insulating film, the pixel electrode and the drain electrode are connected to each other via a second contact hole, and the resistance of the wiring is smaller, so that the time constant when a signal is written into a holding capacitor via transistor is reduced, such that the drive signal being transferred more fast.

Therefore, the claims 1 and 13 of this application and the claim 8 of the patent US 6,466,280 substantially have the doctrine of obviousness-type double limitations, and they have at least an obviousness-type difference.

Claim 2, the gate line is the first line layer, inherently, the material of the first line layer is the same as the gate line, and that would have been at least obvious.

Claim 3, concerning the limitation such that double-structure gate lines (first line layer), Dojo discloses (col.3, lines 59-67; Fig.2) that the scanning line (111) have a double-layer structure consisting of Aluminum-Neodymium (AlNd) alloy film (1110) and molybdenum (Mo) film (1111). Dojo indicates (col.2, lines 52-68) that due to such multi-layer formation (the scanning line comprised such Al alloy) would lower the wiring resistivity and would have no damage from etching process. Therefore, it would have been obvious to those skilled in the are at the time the invention was made to use AlNd and Mo double layer to form the gate line as claimed in claim 3 for reducing the line resistance and secure the line formation have no damage from the etching process.

Claims 4 and 5, the data line is the second line layer, inherently, the material of the second line layer is the same as the data line, and using metal Cr that is common and known in the art, because the metal Cr has a high corrosion resistance.

Claims 6 and 7, the reflective layer (reflective electrode) is the third line layer, inherently, the material of the third line layer is the same as the reflective layer; and concerning the limitation such that the material of the third line layer, Dojo discloses (col.8, lines 39-42) that the AlNd alloy is a low-resistance material. Therefore, using AlNd alloy as the material of the reflective layer would reduce the line resistance and

the metal material comprising Al alloy having high reflectance, and that is common and known in the art. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use AlNd alloy as the material of the reflective layer as claimed in claims 5 and 6 for reducing the line resistance and having high reflectance.

Claims 8-9 and 14-15, the limitations are only given weight as intended use as the gate line, data line, reflective electrode, and the insulating layers can be used in a reflective LCD or a transflective LCD and that is dependent on the different applications, and that would have been at least obvious.

Claims 10-12 and 16-18, concerning the limitations such that the first insulating layer, the second insulating layer and the passivation layer (third insulating layer) formed on an entire surface of the substrate are covered by the claims 1 and 13 of this application and also are covered by the claim 8 of the patent US 6,466,280.

Response to Arguments

7. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Qi
March 18, 2004

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